

FIG. 1A
PRIOR ART

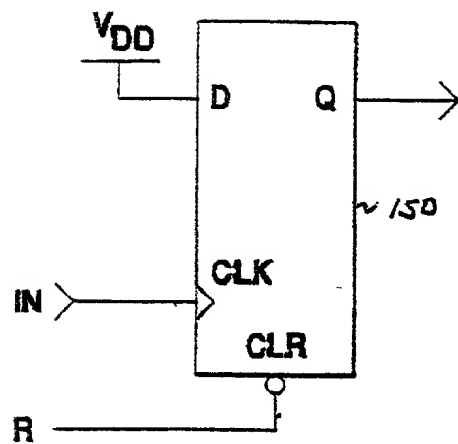


FIG. 1B
PRIOR ART

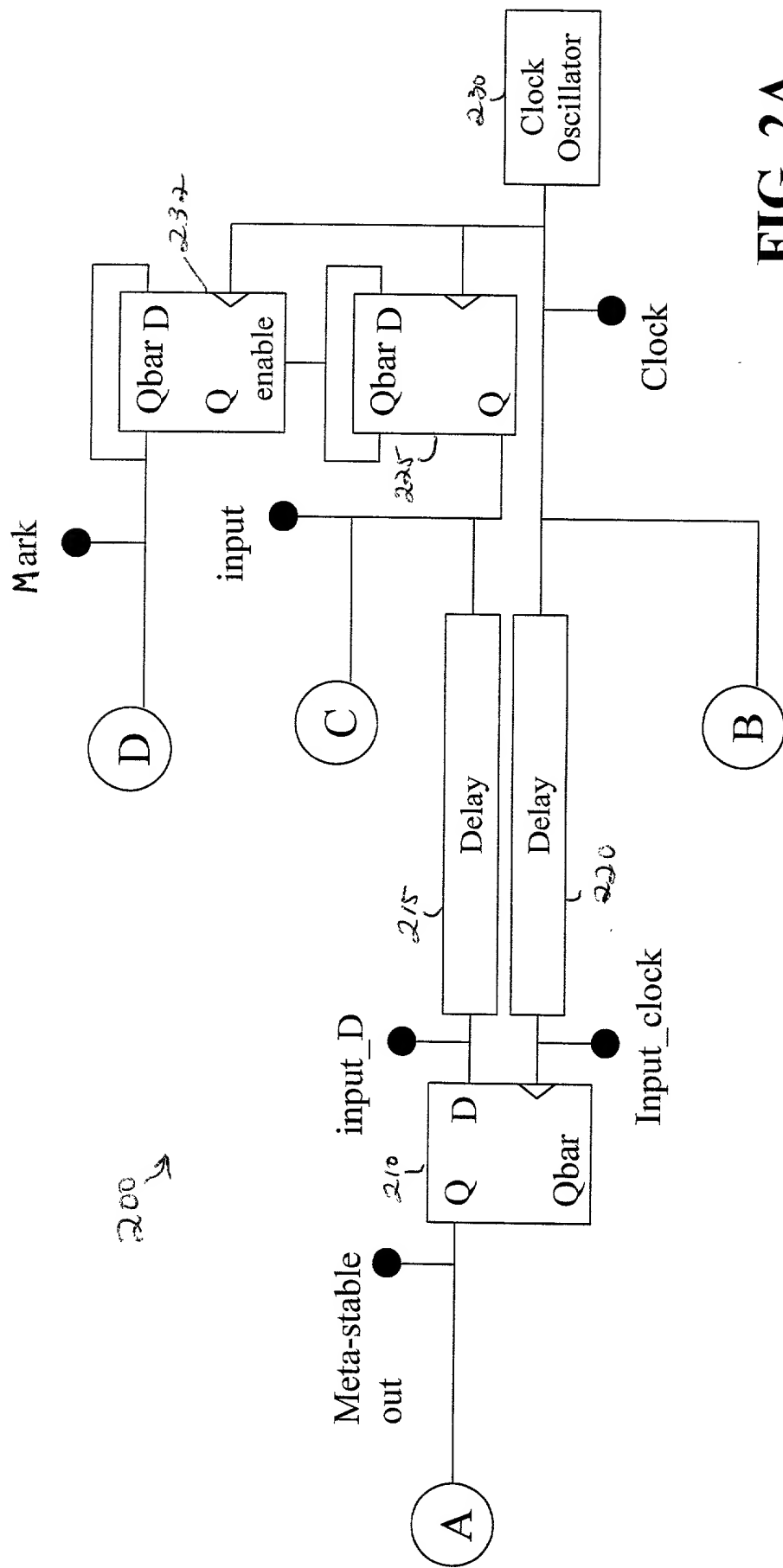


FIG. 2A

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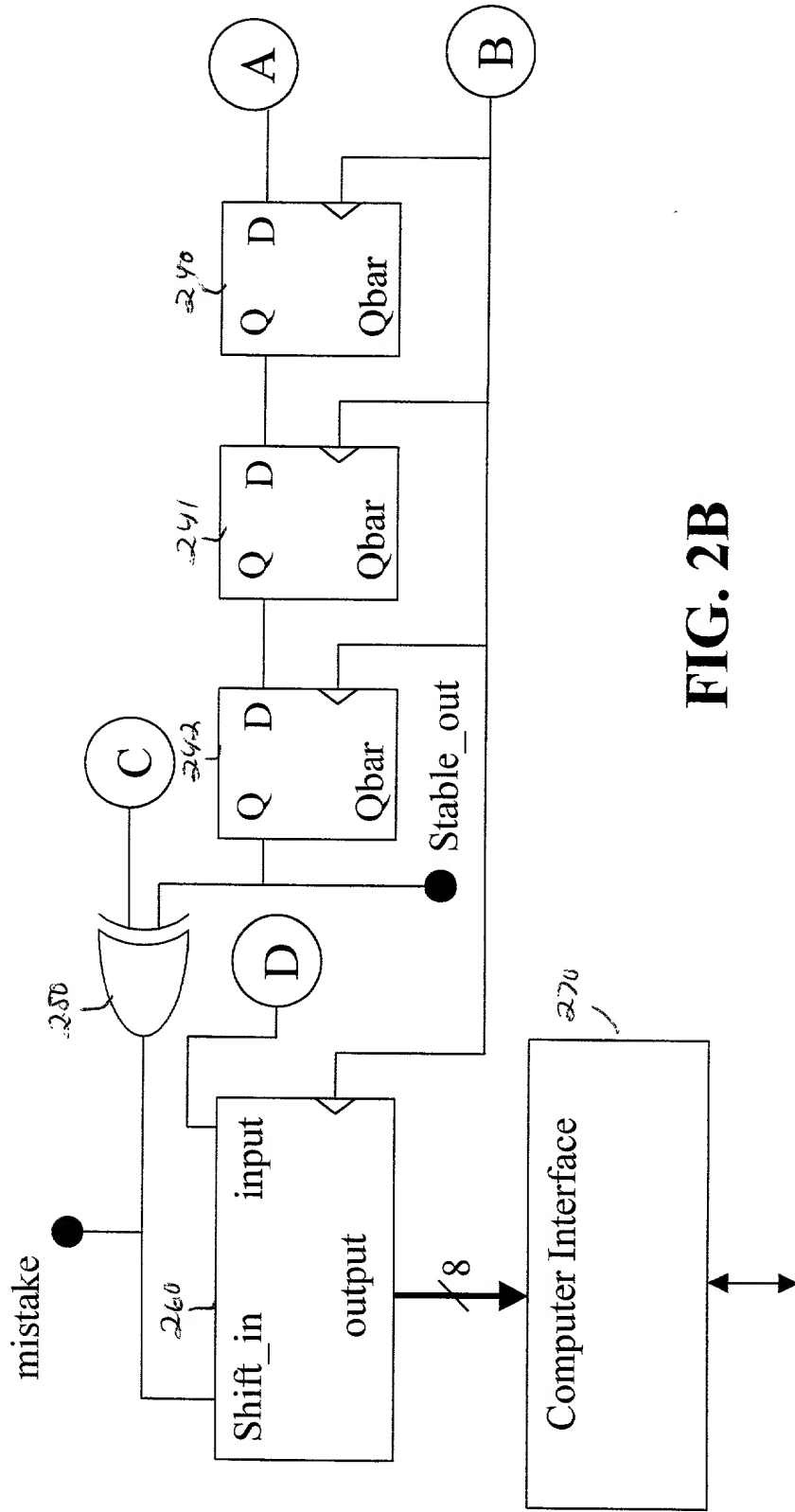
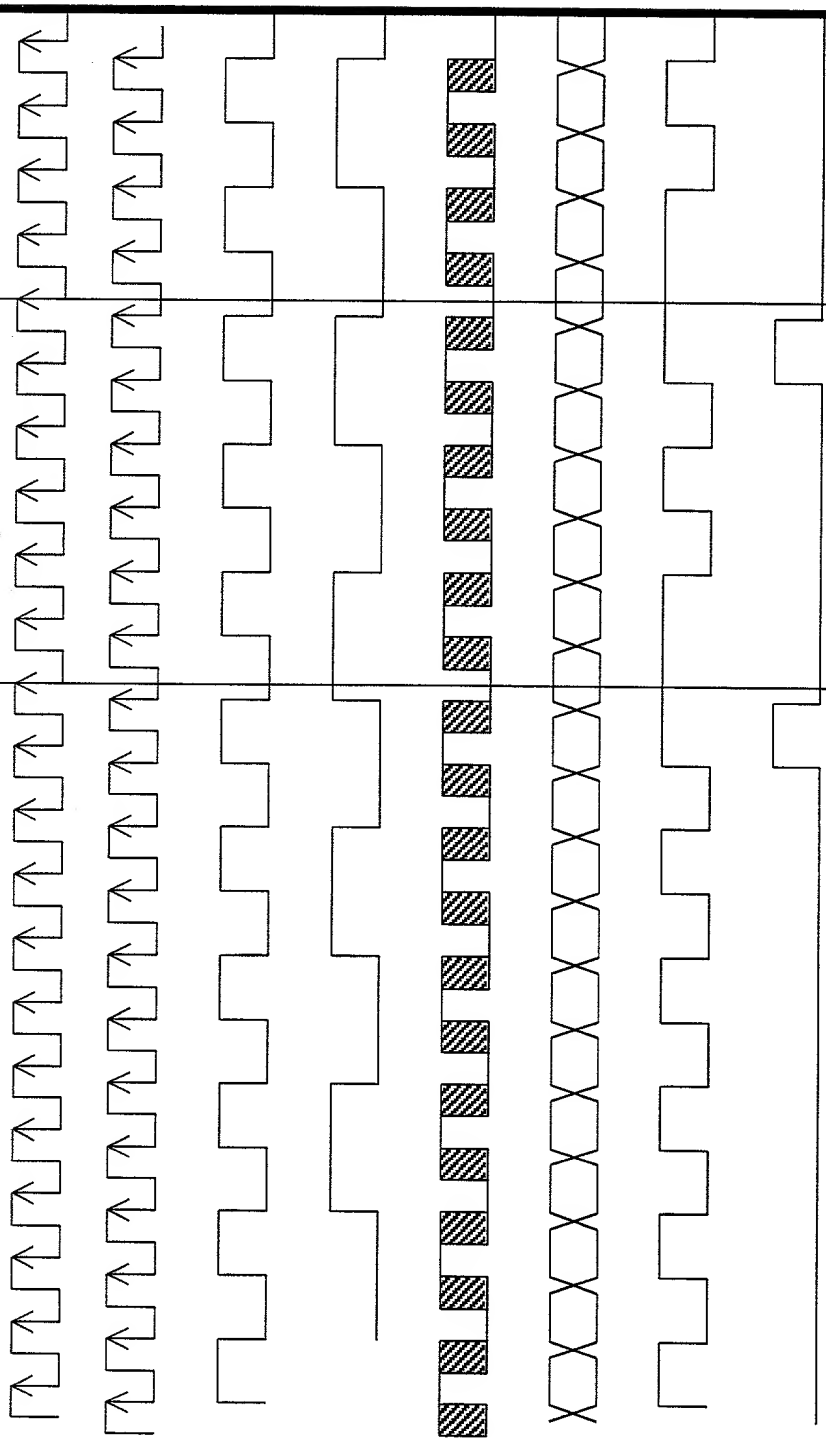


FIG. 2B

FIG. 2C

Clock
Input_clock
Input
Mark
Input_D
Meta-stable out
stable_out
mistake



mistake zero

mistake one

FIG. 2C

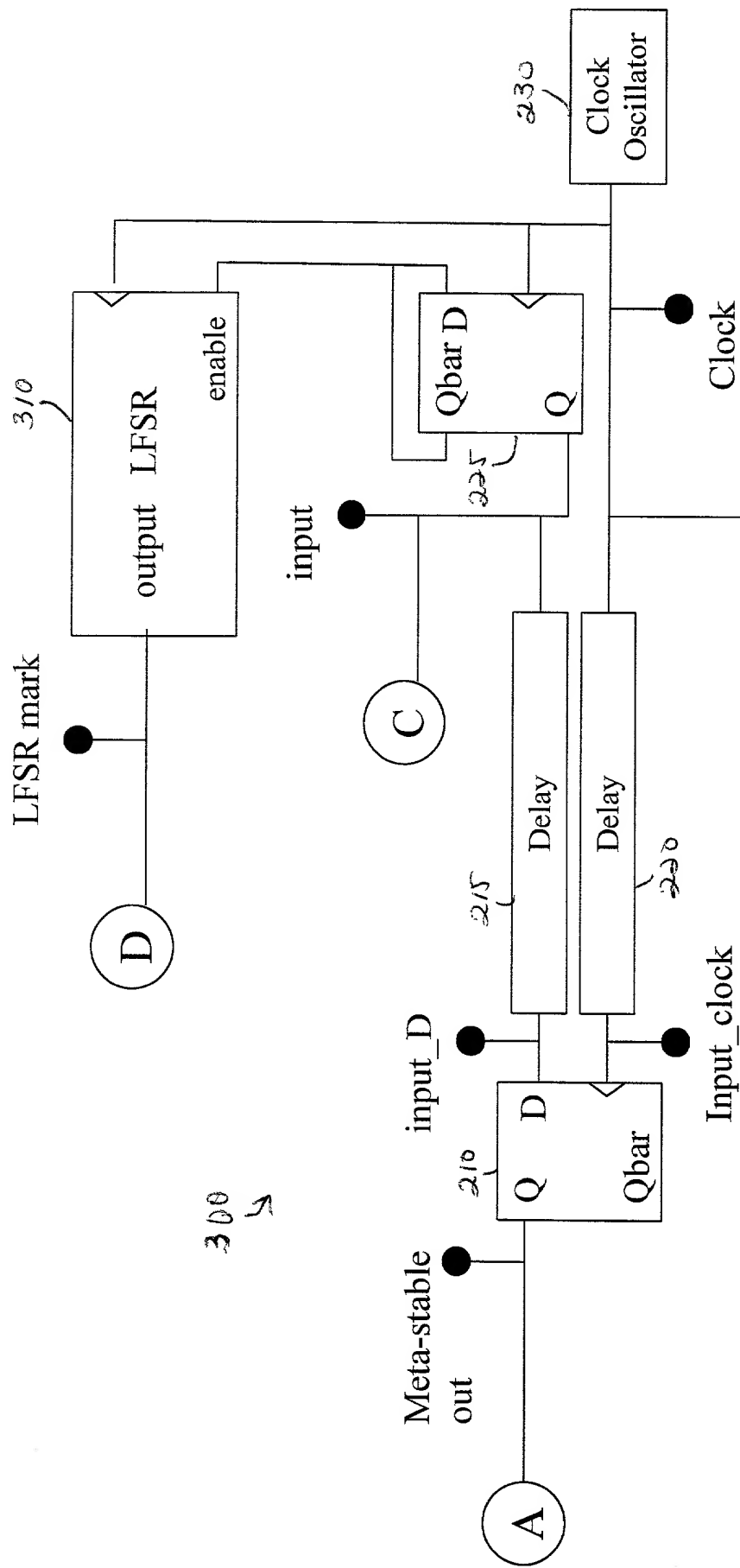


FIG. 3

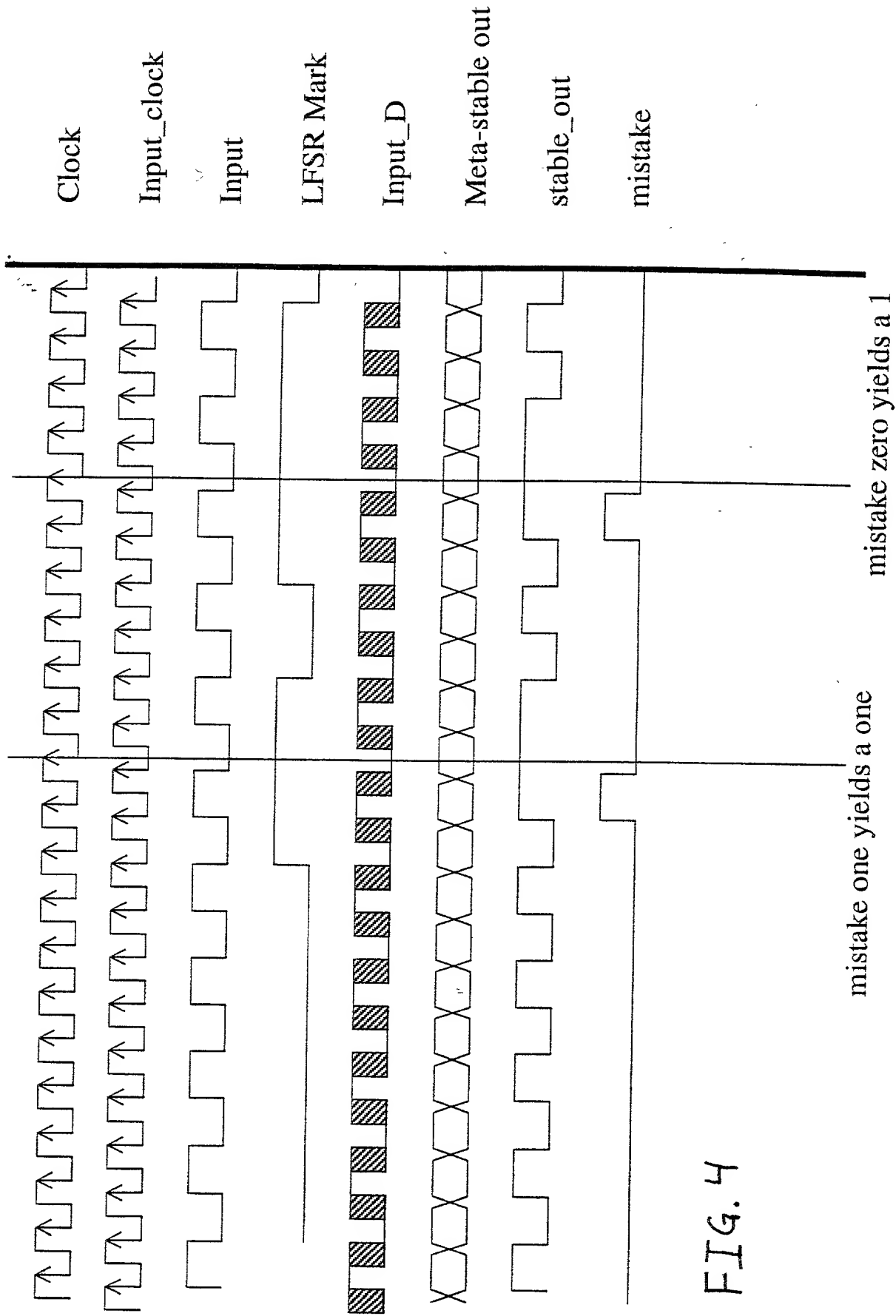


FIG. 5

